Implementation and Prospects for chip-to-chip free-space optical interconnects

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Abstract:
This paper describes the state of the art in free space optical interconnects as applied to chip-to-chip communication. We will review various technologies that integrate micro lasers and optical detectors with silicon CMOS, provide optical link characteristics obtained with these devices, and discuss the capabilities of low cost and robust optoelectronic packaging techniques to seamlessly integrate optics and electronics at the board level.

Introduction
Since the early 1980's optical interconnects have been considered as potential replacements to electrical wires in digital systems within a single cabinet or box. They are targeting first the longest distance communication links ranging from board to board, MCM to MCM, chip-to-chip, and on-chip communications. Early interest on optical interconnects stemmed from the commercial success of optical fiber systems for long haul telecommunication applications as well as from the intrinsic physical advantages offered by photonic transport systems. Photons (Bosons) do not have charge and mass making them better suited for information transport than electrons (Fermions) that suffer from interference, crosstalk and capacitive effects. In addition because of the ultra high frequency of the optical carrier available to them, optical interconnects can in principle offer very high bandwidth (both spatial and temporal). Adverse effects such as reflections and frequency dependent crosstalk that impendence electrical transmission lines can also be easily eliminated.

Optical Interconnects: Status
Both guided wave and free space optical interconnects have been studied extensively for digital systems, particularly for inter and intra-board interconnects and several prototype systems have been successfully demonstrated. In general, guided wave approaches provide ease of implementation and leverage from telecom applications while free-space optical interconnects provide in principle unequaled interconnect density with high optical efficiency.

Significant progress and practical demonstrations of backplane and board to board communication have been made over the last decade using guided wave optical interconnects based on optical fibers or flexible optical waveguides. For example, recently, a fully embedded board-level guided-wave optical interconnection implementing a high speed 1-48 optical clock signal distribution network for Cray T-90 super computer has been demonstrated. Linear arrays of thin-film polyimide waveguides, vertical-cavity surface-emitting lasers (VCSELs), and metal semiconductor-metal (MSM) photodetectors have been integrated. The waveguides included couplers, tilted gratings and 45 degrees total internal reflection mirrors. Waveguide propagation loss under 0.21 dB/cm at 850 nm was achieved for the 1-48 clock signal distribution and for point-to-point interconnects. More recently 3-Gb/s data transmission with GaAs VCSELs over PCB integrated polymer waveguides have been demonstrated at bit-error rates (BERs) of less than 10^-11. If the bit error rate could be lowered further, the implementation of IEEE standard bus protocols as VME bus and FutureBus with such interconnects would become feasible.

Free-Space Optical Interconnects (FSOI) that rely on flip-chip bonded optoelectronic component arrays on CMOS circuits have been mostly studied for board-to-board and chip-to-chip communication. Earlier system demonstrations were based on multiple quantum well absorption modulator arrays used as optical transmitters. However, it is only with the realization of low cost, oxide confined VCSEL arrays and efficient and fast MSM photodetectors arrays fabricated on III-V substrates that FSOI have gained significant practical importance. It can be shown with available devices that FSOI can move data faster and with lower power dissipation at the board level when compared to conventional CMOS driven source-terminated transmission lines (with rail to rail voltage swing) and guided wave solutions that generally suffer from larger optical coupling losses. For example, FSOI can already link two chips a foot apart at 2.5Gb/s per channel by dissipating only a few mW of power from the input of the transmitter driver to the output of the receiver circuit. About 1000 optical I/O pins can be implemented per cm² of chip area.

However, since the voltage available at the output of the optical detectors in such FSOI links is typically only about 100-500µV, signal integrity in FSOI becomes a major concern for their use in computing systems such as backplane applications. For such applications FSOI links need to include additional circuits for signal conditioning.
and error correction reducing their advantage. Fortunately, for applications such as routers for optical datacom and telecom systems, that inherently use signal conditioning circuits and that are starving for bandwidth and interconnect density FSOI may provide an attractive alternative.20,21

Finally, very recently with the advent of photonic crystal structures and their integration on silicon wafers, investigation of optical interconnects for intra-chip communication has been initiated in a limited number of academic institutions. However, many serious hurdles must still be overcome especially in terms of signal integrity, reliability, reduction of optical losses, more efficient electrical to optical power conversion, packaging, and cost considerations before optical on-chip interconnects can be considered to be a viable alternative to very short length electrical wires.

For the next decade however, FSOI has become a potentially viable solution for chip-to-chip interconnects for distances greater than 10cm at speeds exceeding 2.5Gb/s. They are well suited for applications requiring large interconnection density, high distance-bandwidth product, low power dissipation, and low crosstalk at high-speeds. Two major accomplishments have made FSOI significantly more realistic over the last few years: i) the integration at wafer scale of optoelectronic and silicon devices by flip-chip bonding, and ii) the advent of low cost, robust plug-on-top packaging of FSOI with electronics.

Integration of Optoelectronic transmitter/receivers with Silicon CMOS circuits
Heterogeneous integration22 of light emitting devices with silicon CMOS has been a major challenge for chip to chip optical interconnects. Chip level flip-chip bonding of OE devices on CMOS silicon chips has been the mainstream approach but suffered from high cost of integration. Fortunately, with a clever process developed at Honeywell Technology Center, CMOS circuits can now be tightly integrated with micro-laser and detector arrays at moderate cost using wafer scale level flip-chip bonding. As shown in Fig. 1, the process relies on the use of a transparent superstrate to remove the optoelectronic devices from their mother GaAs wafer. Subsequently the superstrate wafer is flip-chip bonded with the CMOS circuits on a silicon wafer. The use of a transparent superstrate enables i) the handling of the optoelectronic devices at wafer scale, ii) the use of eye-safe micro lasers emitting at 850nm where the original GaAs substrate is opaque, and iii) the further integration of the OE devices with passive optical components such as lenslet arrays.

The system demonstrations that are discussed next have used devices that were produced with HTC process yielding micro lasers with 300μA threshold currents and 50% electrical to optical conversion efficiency. In addition, the failure statistics of these devices have been measured to be log-normal leading to reliable array operation.

Fig.1: Process of integrating OE components on Silicon CMOS by means of a superstrate and flip-chip bonding and the eye diagram of an optical link operating at 2.5Gb/s using the process above. (Courtesy of HTC)

Packaging Free Space Optical Chip to Chip Interconnects
Packaging has always presented both a technical and an economical challenge to the manufacturability and cost effectiveness of optical systems. Low cost packaging techniques for FSOI but fully compatible with electronics packaging materials and approaches for both chip-to-chip as well as MCM-to-MCM interconnects have been investigated recently by the 3-D OESP consortium lead by UCSD. As one of the outcomes of this investigation, we have demonstrated a PCB motherboard with 10 free-space optically interconnected chips, which can perform a distributed radix-2-butterfly calculation for fast Fourier transformation (FFT). As shown in Fig. 2, this motherboard includes five multi-chip-modules (MCMs, with processor / transceiver chips and laser/detector chips), and four plug-on-top optics modules that provide the bi-directional optical links between the MCMs. The design of the optics and optomechanics satisfies numerous real-world constraints, such as compact size (< 1 inch thick), suitability for mass-production, suitability for high density (up to 10^2 parallel channels), compatibility with standard electronics fabrication and packaging technology, and robustness to misalignments. Fig.3 shows in greater details one of the optical modules and its optical design. Fig.4 is a photo of the optoelectronic MCM including to silicon processor chips at the center and two VCSEL/MSM array chips for optical transmission and reception.
Fig. 2: Photo of the fully assembled motherboard (40 cm x 20 cm) on its support. Five daughterboards, are interconnected with four optics modules. In the center of the board is the system control FPGA, and in the foreground are three ribbon cables that connect to the external "interface board."

We successfully demonstrated all the steps that are necessary to run the algorithm, such as bi-directional optical MCM-to-MCM communication, data movement within the system and basic arithmetic operations including a number of experiments that showed the robustness of our plug-on-top approach.

Similar demonstrations are under development by several military equipment manufacturers and commercial startup companies.

Fig. 3: Photo of the optics package. Underneath the photo, the CODE V™ simulation drawing of the optics is shown for reference. The package is made from Plexiglas, and is plugged on top of the electronics by means of pinholes and guide pins. The black cylinder in the middle of the setup is the mount for the central alignment mirror. The height of the package is 20 mm and total length of the top plate is 146 mm. Each module operated with 90% optical efficiency and -40dB channel isolation.

Fig. 4: Photo of a multi-chip-module (daughterboard) that holds two processor chips (in the middle, and two OE chips chips (left and right, for communication from and to the left and right neighbor). The size of the board is 80 mm x 40 mm.

As a second demonstration of the capabilities FSIO for MCM to MCM communication, we describe next a crossbar switch capable of 256 optical I/O channels, 1Gb/s data rate per channel and configuration times approaching a few tens of nanoseconds in a footprint area of approximately 100cm².

Towards this goal, we have developed a scalable 3-Dimensional Optical Interconnect Distributed Crossbar Switching (3DOCS) architecture depicted in Fig.5. In this architecture, M x N x k Xbar switches are stacked in a third spatial dimension and data is delivered to/from the crossbar via optoelectronic I/Os. Not only does the distributed OE approach reduce the footprint area requirements of the two-dimensional crossbar by O(N), but it also enables a substantial bandwidth increase.

Fig. 5: 3D Distributed Crossbar Switching architecture

Fig. 6: System architecture of 3DOCS

At the core of this design are three optoelectronic VLSI chip-stack modules (or 3D-MCM) as shown in figure 6. These chip stacks are interconnected via an FSIO layer. Each chip-stack (14 x 14 x 9 mm) consists of 16 VLSI chips. The high-speed data I/O to each stack is achieved via one 16 x 16 VCSEL/MSM array, which is bump bonded onto the top of each stack. The control of the stack is performed electrically at lower speeds. Each VLSI chip in a stack, fabricated by the HP AMOS14TB process (0.35um), includes four 16 x 16 crossbar switches operating at 250 Mb/s, with 64 electronic I/Os. Using a MUX/DEMUX circuit these I/Os are interfaced with the 16 optoelectronic I/Os each operating at 1 Gb/s. Thus the data I/O rate of a chip stack when accessed optically is 256Gb/s. The transmitters of the optoelectronic I/Os are implemented in current-mirror style, and the receivers have transimpedance amplifier based design. On-chip crossbar switches are modified-mux style and special circuitry to assure synchronized I/O. The chips are integrated into stacks of 16 chips by Irvine Sensors. The VCSEL/MSM array with 500µm device pitch is fabricated and bump bonded onto the silicon stacks by Honeywell Technology Center.
The optical interconnect layer is a hybrid one-to-one imaging system, which includes micro-lenses to collimate and focus, diffraction gratings to redirect the beams and refractive lenses to image. This system is optimized to provide sufficient lateral and longitudinal misalignment tolerances for final assembly and operates with 80% optical power efficiency. As shown in Fig.8, the OE I/O of the chip stacks operate at 1Gb/s.

In conclusion, we believe that for future high-speed router and large switch implementations, FSOI offer a unique physical solution with compact and affordable optics modules in sight. Although the chosen approach of packaging optics on top of existing electronics produced good results, we think that optics and electronics should further share the burden. Possible improvements on the electronic side include for example rigid PCBs that can serve as an optics "breadboard", precise pick-and-place machines that allow for cheap assembly of optoelectronic parts, or array-layouts that respect the rotational symmetry of many optical imaging systems.

References: